CLAIMS

1. A signal flow driven circuit analysis technique by tracing circuit signal flow so that, analyzing a circuit, and partitioning a circuit based on functionality and criticality, and generating multitude circuit layout constraints are done by software program automatically.

2. A signal flow driven circuit physical synthesis technique by tracing circuit signal flow so that, placing and routing circuit cell physical layout based on giving critical signal path with high priority are done by software program automatically.

3. A signal flow driven circuit physical synthesis technique of claim 2 comprising:
   (a) Providing a memory that is able to store a circuit netlist employing input and output pins, any other terminal pins, power and ground terminals, active device elements, and passive device elements; and
   (b) Storing said circuit netlist in said memories; and
   (c) Providing a memory that is able to store a series of technology files in said memory; and
   (d) Storing said series of technology files in said memory; and
   (e) Providing a memory that is able to store a series of signal flow information generated from the signal flow driven circuit analysis technique of claim 1 in said memory; and
   (f) Storing said series of signal flow information in said memory; and
   (g) Providing a memory that is able to store said multitude circuit layout constraints generated from the signal flow driven circuit analysis technique of claim 1 and from said signal flow information in said memory, and a series of parasitic loading constraints generated from said signal flow information, and a series of geometry constraint generated from said signal flow information, and a series of proximity constraints generated from said signal flow information in said memory; and

(h) Storing said multitude circuit layout constraints, and said series of parasitic loading constraints, and said series of geometry constraint, and said series of proximity constraints in said memory; and

(i) Providing a memory that is able to store a critical device generator in said memory; and

(j) Storing said critical device generator in said memory; and

(k) Utilizing said circuit netlist, and said series of technology files, and said signal flow information, and said multitude layout constraints, and said parasitic loading constraints, and said critical device generator to synthesize a series of circuit component layouts and a series of unit circuit layouts while observing optimized matching, optimized area, optimized symmetry, and optimized parasitic loading requirements.

4. The signal flow driven circuit physical synthesis technique of claim 2 further including a signal flow driven circuit cell placement methodology comprising:

(a) Providing a memory that is able to store a placement module in said memory; and

(b) Storing said placement module in said memory; and

(c) Providing a memory that is able to store a series of matching requirements of a series of devices associated with a critical signal flow path and a series of symmetry requirements of said series of devices associated with said critical signal flow path in said memory; and

(d) Utilizing said placement module and the signal flow driven circuit physical synthesis technique of claim 3 wherein said series of circuit component layouts and wherein said series of unit circuit layouts to layout said circuit providing minimized separations of the circuit component layouts and the unit circuit layouts in said critical signal flow path; and

(e) Utilizing said placement module to place a series of non-critical components in rest of said area; and

Whereby an engineer can achieve compact layout for an analog circuit, a mixed signal circuit, and a RF circuit automatically.

5. The signal flow driven circuit physical synthesis technique of claim 2 further including a signal flow driven circuit cell routing methodology comprising:
   (a) Proving a memory that is able to store a routing module in said memory; and
   (b) Storing said routing module in said memory; and
   (c) Providing a memory that is able to store a series of parasitic loading constraints of multitude circuit nodes of a critical signal flow path in said memory; and
   (d) Utilizing said routing module, and said series of parasitic loading constraints, and the signal flow driven circuit physical synthesis technique of claim 3 wherein said geometry constraints and said proximity constraints to connect a series of critical nets in said critical signal flow path of said circuit before connecting a series of non-critical nets in said circuit; and

Whereby an engineer can route an analog circuit, a mixed signal circuit, and a RF circuit automatically.

6. A mean of circuit performance assurance utilizing:
   (a) The signal flow driven circuit analysis technique of claim 1; and
   (b) The signal flow driven circuit physical synthesis technique of claim 2; and
   (c) The signal flow driven circuit cell placement methodology of claim 4; and
   (d) The signal flow driven circuit cell routing methodology of claim 5.

7. A mean for circuit physical layout floor planning utilizing:
   (a) The signal flow driven circuit analysis technique of claim 1; and
   (b) The signal flow driven circuit physical synthesis technique of claim 2; and
   (c) The signal flow driven circuit cell placement methodology of claim 4; and
   (d) The signal flow driven circuit cell routing methodology of claim 5.

8. A mean of incorporating an in-situ parasitic extraction process having the signal flow driven circuit cell routing methodology of claim 5 wherein said routing module incorporated in said in-situ parasitic extraction process.